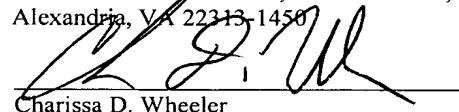


Sole Inventor

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Charissa D. Wheeler

## APPLICATION FOR UNITED STATES LETTERS PATENT

## S P E C I F I C A T I O N

TO ALL WHOM IT MAY CONCERN:

Be it known that I, Kwan-Ju KOH, a citizen of Republic of Korea, residing at 407-101 Keumkang Maeul, Jung 4-dong, Wonmi-ku, Bucheon-city, Kyungki-do 420-729, Republic of Korea have invented a new and useful **METHODS OF FABRICATING NON-VOLATILE MEMORY DEVICES**, of which the following is a specification.

## METHODS OF FABRICATING NON-VOLATILE MEMORY DEVICES

### TECHNICAL FIELD

**[0001]** The present disclosure relates to a semiconductor devices and, more particularly, to methods of fabricating non-volatile memory devices.

### BACKGROUND

**[0002]** In general, semiconductor memory devices are roughly classified into volatile memory devices and non-volatile memory devices. Most of the volatile memory devices are random access memory (RAM) such as dynamic random access memory (DRAM), static random access memory (SRAM), etc. Volatile memory devices are devices that, when power is supplied to the volatile memory, it is possible to input and preserve data, but, when power to the volatile memory is interrupted, the information therein is lost.

**[0003]** Conversely, most of the non-volatile memory devices are read only memory (ROM), and thus it is possible to preserve data even when power to the device is interrupted.

**[0004]** Currently, on the process technology side, the non-volatile memory device is classified into a floating gate group and a metal/insulator/semiconductor (MIS) group in which dielectric films of two or more types are layered to be two or three floor.

**[0005]** The non-volatile memory device of the floating gate group stores data using potential well, and currently, the representative structure thereof is an EPROM tunnel oxide (ETOX) structure that is widely applied to an electrically erasable programmable read only memory (EEPROM).

**[0006]** On the other hand, the non-volatile memory device of the MIS group memorizes data using traps that exist in dielectric film bulk, an interface between dielectric films, and an interface between a dielectric film and a semiconductor. Currently, the representative structure thereof is a metal/silicon ONO semiconductor (MONOS/SONOS) structure that has been used as an EEPROM.

**[0007]** Conventional arts relating to a flash memory having the SONOS structure are disclosed in U.S. Patents 6,440,797; 6,444,545; 5,424,569; and 5,387,534.

**[0008]** Fig. 1 is a cut view showing a non-volatile memory device having a conventional SONOS structure, and, as shown in Fig. 1, phosphorus is injected into a semiconductor substrate 1 to form a first semiconductor region 2, and an ONO layer 3 having a oxide/nitride/oxide laminated structure is formed thereon, and then polysilicon layer 4 is formed on the ONO layer 3, such that the SONOS structure of a semiconductor/ONO/semiconductor structure is accomplished.

**[0009]** In a method of fabricating a non-volatile memory device having such conventional SONOS structure, because a photo-engraving process has to be carried out repeatedly, there is a problem of complicated process, much manufacturing time, and much cost to manufacture.

#### BRIEF DESCRIPTION OF THE DRAWINGS

**[0010]** Fig. 1 is a cut view showing a conventional non-volatile memory device.

**[0011]** Figs. 2a to 2f are cut views showing the results of an example method of fabricating non-volatile memory device.

#### DETAILED DESCRIPTION

**[0012]** Figs. 2a to 2f are cut views showing a method of fabricating non-volatile memory device according to the present invention.

**[0013]** First, as shown in Fig. 2a, a sacrificial oxide film 12 is formed on a silicon wafer 11, and a first photo engraving process is carried out to selectively etch the sacrificial oxide film 12, and the etched portion of the silicon wafer 11 is exposed.

**[0014]** At this point, the sacrificial oxide film 12 is etched to have proper size and width in consideration of fact that SONOS device will be formed in a portion of the sacrificial oxide film 12 that is to be etched subsequently, and in the same manner, deposition thickness of the sacrificial oxide film 12 is also decided to be proper size for the SONOS device.

[0015] Subsequently, as shown in Fig. 2b, an additional oxide 14 and a nitride film 15 are laminated on the entire upper surface of the sacrificial oxide film 12 including the exposed silicon wafer 11 to form an ONO layer.

[0016] Then, photoresistive film is applied on the nitride film 15, and then exposure and development processes are carried out to form a photoresistive film pattern 16 for forming a gate.

[0017] Next, as shown in Fig. 2c, the exposed nitride film 15, a second photo engraving process is carried out to etch the additional oxide 14, and the sacrificial oxide film 12 using the photoresistive pattern 16 as a mask, and thus the silicon wafer 11 is exposed through the etched portion.

[0018] Subsequently, a gate oxide film 17 is formed over the entire upper surface of the silicon wafer 11, and then polysilicon layer 18 is formed thereon thickly.

[0019] At this point, the polysilicon layer 18 is completely filled in a portion etched through the second photo engraving process, and the filled polysilicon layer 18 functions as a gate. Thus, the polysilicon layer, which will function as a gate, is formed using a burying method, i.e., a damascene process.

[0020] Next, as shown in Fig. 2d, the chemical mechanical polishing (CMP) process is carried out to flat the upper surface until the sacrificial oxide film is exposed. At this point, the etching process is closed at the point of time when the nitride film 15 is exposed using the nitride film 15 as a polishing stopper layer, and then the sacrificial oxide film 12 is exposed by carrying out over-etch for a predetermined time.

[0021] Then, as shown in Fig. 2e, a gate oxide film 17, the nitride film 15, and the additional oxide 14 formed on the side walls of the sacrificial oxide film 12 and the polysilicon layer 18 are removed using a wet-etch.

[0022] Then, as shown in Fig. 2f, a protection film 19 is formed over the entire upper surface of the silicon wafer 11, and then a second conductive type impurity ions, the conductive type of which is opposite to the first conductive type impurity ions injected into the first semiconductor region 13, is injected into the silicon wafer

11 using the polysilicon layer 18 as a mask to form a lightly doped drain (LD) region.

**[0023]** Subsequently, the side-walls 20 are formed on the protection film 19 located on the side walls of the polysilicon layer 18, the gate oxide film 17, the nitride film 15, and the additional oxide 14, and then, impurity ions, which has the same conductive type as the second conductive type impurity ions injected into the LDD region, is injected into the silicon wafer 11 using the side-walls 20 and the polysilicon layer 18 as a mask to from source and drain regions 21, such that the non-volatile memory device having the SONOS structure comes to be fabricated.

**[0024]** As described above, in the example disclosed method, the non-volatile memory device having the SONOS structure can be fabricated using the photo engraving process only twice. According to the example method, a gate is formed using the damascene process, and thus the non-volatile memory device having the SONOS structure can be fabricated using the photo engraving process only twice, such that the process therefore can be simplified and the cost and the time required for fabrication can be decreased.

**[0025]** According to one example method, the method includes forming a sacrificial oxide film on a semiconductor substrate and selectively etching the sacrificial oxide film to expose the semiconductor substrate with a predetermined width; injecting first conductive type impurity ions into the exposed semiconductor substrate to form a first semiconductor region, forming an additional oxide and nitride film on the entire upper surface of the semiconductor substrate in order; selectively etching the nitride film, the additional oxide, and the sacrificial oxide film to form a gate window which exposes the semiconductor substrate with a predetermined width; forming a gate oxide film over the entire upper surface of the semiconductor substrate; forming polysilicon layer on the gate oxide film to fill in the gate window; carrying out a CMP (Chemical Mechanical Polishing) process until the sacrificial oxide film is exposed; removing the sacrificial oxide film, and the gate oxide film film, the nitride film, and the additional oxide formed on the side wall of the polysilicon layer; injecting second conductive type impurity ions into portions of the

semiconductor substrate, which corresponds to the outer part of the polysilicon layer, to form source and drain regions.

**[0026]** Although a preferred embodiment of the present invention has been described in detail hereinabove, it should be clearly understood that many variations and/or modifications of the basic inventive concepts herein taught which may appear to those skilled in the present art will still fall within the spirit and scope of the present invention, as defined in the appended claims.